Amendments to the Specification

In the Abstract, please amend as shown.

~~A trench-gate transistor (1) has an integral first layer of silicon dioxide (31) which extends from the upper surface (10a) of the semiconductor body (10) over top corners of each cell array trench(20), the integral first layer also providing a thin gate dielectric insulating layer (31A) for a thick gate electrode (41) and the integral first layer also providing a first part (31B) of a stack of materials which constitute a thick trench sidewall insulating layer (31B,32,33) for a thin field plate (42), a layer of silicon nitride (32) providing a second part of the stack and a second layer of silicon dioxide (33) providing a third part of the stack. The integrity of the first silicon dioxide layer (31) over the trench (20) top corners helps to avoid gate (41) - source (24) short circuits. In a method of manufacture (Figures 2A to 2F) a hardmask (21) used to etch the trenches (20) is removed before providing the silicon dioxide layer (31), which layer (31) is then protected by successive selective etching of the oxide layer (33) and the nitride layer (32) in the upper parts of the trenches (20). After the gate electrodes (41) are provided, layers for the channel accommodating regions (23) and source regions (24) may be formed through the oxide layer (31) on the upper surface (10a).~~

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Thanks,
T. D.
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A trench-gate transistor has an integral first layer of silicon dioxide extending from the upper surface of the semiconductor body over top comers of each cell array trench. The integral first layer also provides a thin gate dielectric insulating layer for a thick gate electrode and the integral first layer also provides a first part of a stack of materials which constitute a thick trench sidewall insulating layer for a thin field plate. Consistent with an example embodiment, there is a method of manufacture. A hardmask used to etch the trenches is removed before providing the silicon dioxide layer. The layer is then protected by successive selective etching of the oxide layer and the nitride layer in the upper parts of the trenches. After the gate electrodes are provided, layers for the channel accommodating regions and source regions may be formed through the oxide layer on the upper surface.